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APPLICATION NO:	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/703,335	10/31/2000	Viktors Berstis	AUS9-1999-0269-US1	3082

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EXAMINER
LINDINGER, MICHAEL L

ART UNIT	PAPER NUMBER
2841	

DATE MAILED: 04/23/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/703,335	BERSTIS ET AL.	
	Examiner	Art Unit	
	Michael L. Lindinger	2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-45* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *32-40* is/are allowed.

6)☒ Claim(s) *1-25,27-30 and 41-45* is/are rejected.

7)☒ Claim(s) *26 and 31* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

1. Claim 1 is provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over Claim 1 of copending Application No. 09/703,334. Although the conflicting claims are not identical, they are not patentably distinct from each other because discloses a time cell, which experiences a transition of states after a programming (charging) operation, detections means for detecting a value within a charge storage element, which is located within the time cell. An explicit obviousness statement is not necessary when the Claims are worded almost identically to one another.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims 1-17, 24-25, 41-42, 44-45 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sakaki U.S. Patent No. 5,500,834 in view of Feddeler U.S. Patent No. 5,323,066. Regarding Claims 1-4, 41-42, and 44-45, Sakaki teaches a horological device for measuring the time lapse after a turn off of a power source, wherein a capacitor is charged when power supplied to the system is turned on, wherein the capacitor is discharged when the power is disconnected, wherein the voltage of the capacitor is read (by reading/coupling means) and recorded by a processor, which then interprets and converts information appropriately when the power is turned, wherein the capacitor's value is also read and recorded when the power is turned off, wherein a corresponding time lapse is recorded, wherein inherently this teaches a time detection unit for processing a time request to generate a time response after reading the capacitor's value, thereby measuring the electrostatic charge of the capacitor, wherein the above mentioned elements combine to form claimed time cell (Col. 1, lines 10+; Col. 2, lines 25+; Col. 3, lines 1+; Col. 4, lines 5+; FIG. 1). Sakaki does not teach a horological device comprising a floating gate in a floating gate field effect transistor

(FGFET), explicit time determining means, or the length of a predetermined time period varies with an initial condition of the time cell after the charging operation, wherein the initial condition is determined by an initial electrical potential of the charge storage element. Feddeler teaches a data acquisition means that comprising a capacitor that is replaced with a floating gate in a floating gate field effect transistor (FGFET) (Col. 4, lines 12+; FIG. 5). It would have been obvious to a person skilled in the art at the time of the invention to not only adapt the Sakaki reference and include a floating gate in a floating gate field effect transistor (FGFET) in place of a capacitor in order to further insulate the charge element that is being charged and discharged, but to recognize that any capacitive timing device must inherently possesses the structure and means to read and interpret data as to whether or not a predetermined time period has elapsed in order to verify the time at which to charge the time cell again, as well as to recognize the length of the predetermined time period may be altered by varying the insulating medium after the charging operation, wherein by altering this thickness, initial electrical potential of the charge storage element is directly impacted. Sakaki teaches all of the necessary structure, the methods of charging a charge storage element within controlling electrostatic discharge during and after discharging and charging states of a time cell in order to gain measurement of the elapsed time of the system and the corresponding charging and read operation steps needed to initialize and process the information of the apparatus are inherently possessed within said structure.

Regarding Claims 5-7, the combination of Sakaki and Feddeler references teaches a time cell, which has the ability of a conventional RC timer to measure electrostatic discharge in order to measure elapsed time. The Sakaki/Feddeler combination does not explicitly teach an array of time cells, or the time periods of the time cells in the array of time cell. It would have been obvious to a person skilled in the art at the time of the invention to provide an array of time cells comprising individual time periods whose values maybe the same or different, since it has been held that the mere duplication of parts for a multiplied effect, in the instant an array of time cells for various time measurements, is an obvious improvement (*In re Harza*, 274 F.2d 669, 671, 124 USPQ 378, 380 (CCPA 1960)).

Regarding Claims 8-9 and 24-25, the combination of the Sakaki and Feddeler references teaches a time cell, which has the ability of a conventional RC timer to measure electrostatic discharge in order to measure elapsed time. The Sakaki/Feddeler combination does not explicitly comprise a time cell interface unit, programming request unit, or a status-generating unit for initializing or setting one or more time cells, as well as generating status from the time cells. It would have been obvious to a person skilled in the art at the time of the invention to recognize that any capacitive timing device must inherently possesses the structure and means to charge/discharge time cells, as well as the ability to determine during the charging process whether the cells were successfully charged or not. By including a time cell interface unit and a programming request unit, existing initialization structure of a typical RC timer is applied to the specific invention.

Regarding Claims 10-13, the combination of the Sakaki and Feddeler references inherently possess the methods of controlling electrostatic discharge during and after discharging and charging states of a time cell in order to gain measurement of the elapsed time of the system and the corresponding charging and read operation steps needed to initialize and process the information of the apparatus. It would be obvious to a person skilled in the art at the time of the invention to recognize that because the combination of the Sakaki and Feddeler references form the structure of the inventive entity claimed, the methods needed to construct, charge, and read the components and data contained and produced are inherently possessed by the structure.

Regarding Claims 14-17, it would be obvious to a person skilled in the art at the time of the invention to construct a computer program to perform the method steps of Claims. It is well known in the art to build a computer program on a computer readable medium such as a floppy disk for easy insertion and data recall during use on a computer.

Regarding Claim 43, the combination of the Sakaki and Feddeler references teaches a time cell, which has the ability of a conventional RC timer to measure electrostatic discharge in order to measure elapsed time. The Sakaki/Feddeler combination does not explicitly teach an article of manufacturing comprising a smart card. It would be obvious to a person skilled in the art at the time of the invention to adapt a smart card to include a charge storage device, e.g. an RC timer device in order to measure elapsed time of a

charged storage element with a smart card in order to calculate the elapsed time memory has been stored on a smart card. Any capacitive timing device possesses memory and means to store and read the memory and by applying this concept of measuring electrostatic discharge to calculate memory, a user may read the elapsed time a portion of memory that has been stored on the smart card and recharge or update the memory before it is erased.

3. Claims 18-23 and 27-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sakaki U.S. Patent No. 5,500,834 in view of Feddeler U.S. Patent No. 5,323,066 in further view of the Admitted Prior Art. Regarding Claims 18-23 and 26-31, Sakaki teaches a horological device for measuring the time lapse after a turn off of a power source, wherein a capacitor is charged when power supplied to the system is turned on, wherein the capacitor is discharged when the power is disconnected, wherein the voltage of the capacitor is read (by reading/coupling means) and recorded by a processor, which then interprets and converts information appropriately when the power is turned, wherein the capacitor's value is also read and recorded when the power is turned off, wherein a corresponding time lapse is recorded, wherein inherently this teaches a time detection unit for processing a time request to generate a time response after reading the capacitor's value, thereby measuring the electrostatic charge of the capacitor, wherein the above mentioned elements combine to form claimed time cell (Col. 1, lines 10+; Col. 2, lines 25+; Col. 3, lines 1+; Col. 4, lines 5+; FIG. 1). Sakaki does not teach a horological device comprising a floating gate in a floating gate field

effect transistor (FGFET), explicit time determining means, or the length of a predetermined time period varies with an initial condition of the time cell after the charging operation, wherein the initial condition is determined by an initial electrical potential of the charge storage element, nor does Sakaki explicitly teach the specific structural components described in the Claimed invention. Feddeler teaches a data acquisition means that comprising a capacitor that is replaced with a floating gate in a floating gate field effect transistor (FGFET) (Col. 4, lines 12+; FIG. 5). The Admitted Prior Art teaches a horological device comprising all of the structural features shown in FIGURE 1A: a semiconductor substrate 102, a source region 104, a drain region 106, a channel region 122 between the source region and the drain region, a control gate 116, a floating gate 118 between the control gate and the channel region, wherein the floating gate behaves as a charge stored element in a floating gate field effect transistor (FGFET), wherein an internal medium is provided within the charged storage element to receive programming operations, hereafter referred as charging operations, an insulating medium 120 surrounding the internal medium, wherein the insulating medium has a tunneling region for discharging an electrostatic charge, wherein said insulating medium has physical properties which affect the rate of discharge in a discharge process, wherein one of these physical properties is the thickness of the insulating medium. The discharge process is a non-linear Fowler-Nordheim tunneling process and the charging process is a channel hot electron injection process, which comprising a charge injector for injecting said charge into charge storage element, further comprises a programming unit, hereto referred to as a charging unit for charging the charge

storage element. It would have been obvious to a person skilled in the art at the time of the invention to not only adapt the Sakaki reference and include a floating gate in a floating gate field effect transistor (FGFET) in place of a capacitor in order to further insulate the charge element that is being charged and discharged, but to recognize that any capacitive timing device must inherently possesses the structure and means to read and interpret data as to whether or not a predetermined time period has elapsed in order to verify the time at which to charge the time cell again, as well as to recognize the length of the predetermined time period may be altered by varying the insulating medium after the charging operation, wherein by altering this thickness, initial electrical potential of the charge storage element is directly impacted, wherein including the components of the Admitted Prior Art improves the apparatus' ability to control the amount of electrostatic discharge through the control and floating gates, as well as the tunneling region. Sakaki teaches all of the necessary structure, the methods of charging a charge storage element within controlling electrostatic discharge during and after discharging and charging states of a time cell in order to gain measurement of the elapsed time of the system and the corresponding charging and read operation steps needed to initialize and process the information of the apparatus are inherently possessed within said structure. Also, the Admitted Prior Art comprises read operations that provide a read operation voltage, which is analyzed in order to provide an indication that the floating gate has been charged, therefore in essence detecting an electrical potential within the internal medium and processing the information.

Allowable Subject Matter

1. Claims 26 and 31 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

2. Claims 32-40 allowed.

Response to Arguments

1. Applicant's arguments filed March 27, 2003 have been fully considered but they are not persuasive. The Applicant's argument's regarding the difference between a floating gate field effect transistor, which is utilized in the current invention, and an insulated gate field effect transistor, which is cited in the Prior Art, is noted and persuasive, and this argument is further noted with the allowance of the Claims stated in the Allowable Subject Matter portion of the rejection. However, the remainder of the Claims that are not drawn to or having a floating gate field effect transistor continue to be rejected based on the cited Prior Art. For the foregoing reasons, Claims 1-25,27-30 and 41-45 continue to be anticipated by the combination of the Sakaki and Feddeler references. Accordingly, the Examiner's rejection over the combination under 35 U.S.C. 103(a) is upheld.

Further, the Applicant is warned against future Double Patenting issues between Claims, wherein the following Claims are given as an example of particularly related Claims: Claim 37 of Application No. 09/703,334, Claim 41 of Application No. 09/703,335, Claim 26 of Application 09/703,340, and Claim 46 of Application No. 09/703,344, wherein all of the Claims are drawn to a time cell that is to be read. However, more specifically, Claims 26 and 46 of the above highlighted Claims, respectively, are drawn to binary time cells, wherein Claims 37 and 41 of the above highlighted Claims, respectively, are drawn to analog time cells. The Applicant is warned that analog and binary (digital) timekeeping methods and means are interchangeable in the art.

Prior Art

1. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

- Ishibashi U.S. Patent No. 5,374,904 discloses a phase-locked loop circuit having adjustable reference clock signal frequency and filter capacitance compensation.
- Ma U.S. Patent No. 6,067,244 discloses a ferroelectric dynamic random access memory, wherein an FE transistor replaces a capacitor.
- Begin U.S. Patent No. 4,995,019 discloses a time period measuring apparatus wherein time measure is achieved by utilizing a time variable interpose, which comprises components that correspond to an RC circuit.
- Curtis U.S. Patent No. 5,195,061 discloses a practice timer for measuring elapsed time during an activity comprising a variable time constant RC circuit.
- Takeda U.S. Patent No. Re. 35,043 discloses a self-charging electronic timepiece comprising a time constant RC circuit.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael L. Lindinger whose telephone number is (703) 305-0618. The examiner can normally be reached on Monday-Thursday (7:30-6).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Martin can be reached on (703) 308-3121. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7318 for regular communications and (703) 746-7318 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Michael L. Lindinger
Patent Examiner
Art Unit 2841

MLL
April 21, 2003

DAVID MARTIN
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